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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/676,666
Filing Date: September 30, 2003
Appellant(s): OSBORNE, RANDY B.

Gregory D. Caldwell, Reg. No. 39,926
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/28/06 appealing from the Office action mailed 2/10/06.

(1) Real Party in Interest

The real party of interest is Intel Corporation.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Applicant Admitted Prior Art, U.S. Application 10/676,666, hereinafter "Osborne"

U.S. Patent 5,463,590, Watanabe, hereinafter "Watanabe"

U.S. Patent 5,974,501, Shaver, hereinafter "Shaver"

U.S. Patent 6,182,192, Rovati, hereinafter "Rovati"

"NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" Aug. 2002, hereinafter "NEC"

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

1. Claims 14-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter that was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As claims 14 (and 15 being dependant on 14), cites executable code causing the electronic device to "carry out a test of a memory device to determine whether or not the memory device supports ..." a particular set of attributes; however the method necessary to facilitate this is neither sufficiently detailed in the specification, nor sufficiently obvious to enable one of ordinary skill in the art to enable without undue experimentation and/or more specific disclosure of the intended method itself.

Claim Rejections - 35 USC § 103

2. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590) in further view of Osborne (US Application 10/676,666).

As per claims 1-4, Watanabe teaches a multi-bank memory comprised of memory cells organized into arrays of rows and columns, where only one row of

memory cells may be activated to be accessible at a given time; coupled to control logic which controls accesses made to each bank in response to commands received from an external device including a pre-charge command; wherein the banks affected by the command may be individually specified, see figure 2; but does not explicitly teach that the naturally existing independent bank pre-charge enable signals as are depicted within the embodiment as may be analogously exposed at the interface boundary as other similar signals such as address lines have been (considered to be clearly resulting from a conscious decision to correspondingly depict the integration of pre-charge control logic within the example embodiment, not due to a lack of obviousness that this logic and corresponding independent bank pre-charge enable control signals may be analogously alternatively partitioned in a variety of ways). Correspondingly, Osborne acknowledges that "... those skilled in the art will readily recognize that any combination of address signal lines and/or other signal lines (perhaps control lines) may be employed for the purposes of specifying banks(s) affected by a given pre-charge command and/or providing interoperability with existing DDR variants ...", referring to Figure 2b, which similarly depicts bank pre-charge enable signals and functionality as disclosed by Watanabe; see page 13, lines 16-19. Therefore it is considered obvious to one of ordinary skill in the art to enable independent memory bank pre-charge selection by alternatively exposing an independent discrete encoding of such a designation potentially multiplexed with other analogous signals in a variety of analogous ways potentially enabled in alternate forms through the use of conventional programmable configuration mode registers, for the benefit of enabling more direct external control

over the signals and/or behavior naturally inherent within such a device as may be desired for any arbitrary purpose.

As per claim 5, where claim 2 is covered by Watanabe and Osborne above, Osborne teaches by acknowledgement the obviousness of the support of an auto-pre-charge command by citing "As will be familiar to those skilled in the art, a read or write command with auto-pre-charge (a pre-charge command embedded within the read or write command) causes a combination of a read or write operation immediately followed by a pre-charge operation to take place", see page 14 lines 1-2. Thereby it would be obvious to one of ordinary skill in the art to include support of an auto-pre-charge in the control logic of such a memory device, for the benefit of potentially improving the signaling efficiency of it's interface.

3. Claims 6-9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590) and Osborne (US Application 10/676,666), in further view of "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" second edition, as published 10/2002 in English, and 8/2002 in Japanese.

As per claims 6-9 and 11-13, Watanabe and Osborne teach a multi-bank memory comprised of memory cells organized into arrays of rows and columns, where only one row of memory cells may be activated to be accessible at a given time, coupled to control logic which controls accesses made to each bank in response to commands received from an external device including a pre-charge command wherein the banks affected by the command may be individually specified similarly to claims 1-5 above; however does not teach an external memory controller connected to a CPU and

such a memory which may be configured by; where the memory controller further comprises employing at least one prediction algorithm to determine which row must be open in a memory bank in preparation for an upcoming predicted access command and transmitting either an explicit pre-charge command or an implicit pre-charge command to be carried out immediately proceeding that access command. "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teaches such a memory controller connected to a CPU and memory as claimed, see pages 22 and 25. It would be obvious to one of ordinary skill in the art to combine a CPU and memory controller with such a memory for the benefit of enabling their interaction to enable the more efficient memory device access.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590), Osborne (US Application 10/676,666), and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" in further view of Rovati (6,182,192).

As per claim 10, Watanabe, Osborne, and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teach claim 9, but does not teach that the upcoming access command may depend on the predicted state of the a block's line row pre-charge state, and a queue of outstanding memory access requests. Rovati teaches such a memory controller; see figure 3, and abstract lines 1-22. Therefore it would be obvious to one of ordinary skill in the art to combine the two for the benefit of potentially improving the memory transaction performance/efficiency of such a system.

5. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590), Osborne (US Application 10/676,666), and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" in further view of Shaver et al. (5,974,501).

As per claims 14-15, Watanabe, Osborne, and "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teach a controller coupled to both a CPU and memory device, capable of being configured by executable code which may exist on a machine accessible medium, to enable the use of a pre-charge command as similarly claimed in claims 1-5 above; but does not teach a method to test the type of memory present in such a system to determine it's mode(s) of operation, and thereby correspondingly the necessary programmable configuration of a controller to enable a particular mode's subsequent utilization. Shaver et al. teaches that executable code enables a system comprised of such components may test and determine supported modes of operation of such a memory device, and may be subsequently utilized to program the behavior of a controller to utilize that determined mode of operation; see figure 6, and column 1 lines 1-2. It would be obvious to one of ordinary skill in the art to combine the ability to dynamically determine the attributes of the memory devices interconnected to a memory controller for the benefit of being able to more flexibly and efficiently support a broader range of memory devices within a given system.

(10) Response to Argument

Applicant's arguments filed 8/28/06 have been fully considered but are not persuasive.

With respect arguments cited pertaining to the rejection of claims 14-15 under 35 U.S.C. §112; as enablement requires either a clear written description of the method steps and/or structure required to achieve a claimed invention, or for it to be reasonably derived (MPEP 2163, in re Wang) from that disclosed by one of ordinary skill in the art; and although the applicant specifies "what" (i.e. individual bank pre-charge control) is to be tested for utilizing computer executable code, the disclosure is silent on exactly "how" this may be achieved; and thereby in view that one of ordinary skill in the art is considered to understand that testing for a particular feature among a plurality of features which may be simultaneously present utilizing the same set of multiplexed signal lines can yield false positives (as for example: a simple trial sequencing of hypothesized pre-charge control signal lines, followed by read access from a then hypothetically pre-charged bank, can not seemingly reliably determine if the hypothesized pre-charge control signal sequencing actually functionally performed any function, as such a sequencing may simply have been benignly interpreted, and thereby potentially falsely be interpreted as supporting the feature); and thereby in absence of any explicit teachings by applicant otherwise, the claims are not considered enabled without likely undue experimentation in view of that considered reasonably understood by those of ordinary skill in the art.

With respect to the arguments cited pertaining to the rejection of claims 1-5 under 35 U.S.C. §103; as the rejection is based in combination with that acknowledged as prior art by Osborne within the "Background" section of the disclosure citing "It has also become common practice to attempt to reduce both costs and the physical size of

DRAM devices by multiplexing multiple functions onto the various signal inputs and outputs" (per paragraph [002]), and not based upon an instant application of the disclosed invention; and thereby in view that Watanabe teaches that individual banks may be individually pre-charged utilizing distinct signal lines (see figure 2 output signals from control elements 24-25), it is considered obvious that these may be multiplexed through the interface and thereby directly controlled externally in lieu of being controlled internally as taught by Watanabe

With respect to the arguments cited pertaining to the rejection of claim 6-8 under 35 U.S.C. §103; as NEC is considered to teach that a memory controller may issue a pre-charge command across the multiplexed interface, it is considered obvious that such a pre-charge command may designate individual banks in combination with that considered obvious for claims 1-5 as reviewed above.

With respect to the arguments cited pertaining to the rejection of claim 9 and 11-13 under 35 U.S.C. §103; as it is considered obvious that a memory controller may individually specify the banks to be pre-charged as reviewed above, as determination of which banks to pre-charge would be correspondingly inherent, as evidenced by the fact that Watanabe teaching the same (see figure 2, elements 18, 20 and 24-25).

With respect to the arguments cited pertaining to the rejection of claim 10 under 35 U.S.C. §103; the applicant provides no further argument.

With respect to the arguments cited pertaining to the rejection of claims 14-15 under 35 U.S.C. §103; as Shaver teaches that a component may be tested to determine supported features, the applicant's claims are considered obvious in combination with

that reviewed above; as although the applicant claims testing for specific features, the applicant fails to teach a method by which the specific features comprising individual bank pre-charge command support may be ascertained; and thereby not considered patentably distinguishable over the art of record which similarly does not teach how such features may be ascertained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Paul W. Schlie

Conferees:

Donald Sparks (in lieu of Matt Kim)

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